IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jason M. Howard *et al.*	Examiner:	Chat C. Do
Serial No.:	10/071,373	Group Art Unit:	2193
Filed:	February 8, 2002	Docket No.:	884.584US1
Title:	MULTI-THREADED MULTIPLY ACCUMULATOR		
Assignee:	Intel Corporation	Customer Number:	21186

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant respectfully requests review of the final rejection in the above-identified application. No amendments are submitted with this request. This request is being filed with a Notice of Appeal. The review is requested for the reason(s) stated below:

§102 Rejection of the Claims

Claims 8-9, 15-16, and 19-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chip *et al.* (Chip Stearns, *et al.*, *The Coreware Methodology: Building a 200 Mflop Processor in 9 Man Months,* IEEE, 549 (Sept. 1992)). Applicant respectfully traverses the rejection of claims 8-9, 15-16, and 19-23 because Chip *et al.* fails to teach each of the elements included in claims 8-9, 15-16, and 19-23, and so the Office Action fails to state a *prima facie* case of anticipation with respect to claims 8-9, 15-16, and 19-23.

Chip *et al.* discloses operations on ordinate transformations in parallel. However, a disclosure of ordinate transformations in parallel fails to teach interleaved operands, and fails to teach multi-threaded operations, as included in Applicant's claimed invention.

For example, claim 8 recites, "a multiplier coupled to receive interleaved operands and to produce a product; and a multi-threaded accumulator coupled to the multiplier to receive the product." (Emphasis added). In the specification of the present application on page 5, lines 25-29 it states,

> As a result, the operands on nodes 217 and 218 are interleaved between the sets $\{A_i, B_i\}$ and $\{C_j, D_j\}$. Multiplier 232 receives the interleaved operands on nodes 217 and 218, multiplies them, and produces a data

stream on node 102 interleaved between the products (A_iB_i) and (C_jD_j).

Thus, claim 8 recites a multiplier coupled to receive interleaved operands. In contrast, Chip *et al.* on page 550, right hand column at lines 5-12 recites,

> In this case, shown in Figure 2, a 4-stage pipe exists in both the multiplier and the adder. The pipe stages allow the arithmetic cores to operate on four ordinate transformations in parallel. The floating-point multiplier and adder are effectively interleaved, with each stage transforming one coordinate in the vertex. Table 2 shows how the interleaved scheme transposes the order of the operations to match the latency of the architecture. (Emphasis added).

Having a multiplier and adder "effectively interleaved," and transposing the order of the operations to match the latency of the architecture, as disclosed in Chip *et al.*, fails to teach receiving interleaved operands. Receiving interleaved operands involves alternating the input streams in time to the same device such as a multiplier. (*See* e.g. Applicant's specification on page 3, lines 9-12). A disclosure of "effectively interleaving" a multiplier and an accumulator fails to disclose receiving interleaved operands because "effectively interleaving" two devices is not the same as receiving interleaved operands. Chip *et al.* merely shows operations on a series of operands, first including χ and then y, and transposing the order of the operations to match the latency of the architecture, but fails to teach "a multiplier coupled to receive interleaved operands" as recited in claim 8.

Claim 8 also includes a multi-threaded accumulator. In contrast, Table 2 of Chip et al. discloses an entry where "ax + by" is performed in the "Adder Operation". Therefore, any operations including χ and y are combined in the adder of Chip *et al.*, and therefore cannot be multi-threads, as recited in claim 8. Multi-threads are sets of operands that produce different products and are maintained as separate entities throughout the operations performed on these sets of operands as they pass through the multi-threaded accumulator. In Chip et al., operands χ and y are shown as combined in the "Adder Operation," and thus are not multi-threaded as recited in claim 8.

Therefore, Chip *et al.* fails the teach each of the elements of claim 8, and so the Office Action fails to state a *prima facie* case of anticipation with respect to claim 8, and also with respect to dependent claims 9 and 15 that depend from claim 8.

In another example, claim 16 recites, "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads." (Emphasis added). In a further example, claim 23 recites, "the accumulator including sequential elements to provide a multi-threaded capability." (Emphasis added).

As noted above, Chip *et al.* on page 550, in the right hand column at lines 5-7 recites, "in Figure 2, a 4-stage pipe exists in both the multiplier and the adder." However, Chip *et al.* fails to teach the elements of claims 16 and 23 as quoted above because Chip *et al.* goes on to state on page 550, in the right hand column at lines 7-8, "The pipe stages allow the arithmetic cores to operate on four ordinate transformations in parallel." (Emphasis added).

Therefore, with regards to claims 16, the four separate registers relied on in the Office Action mailed September 9, 2005 on page 4 represent registers operating in parallel on four ordinate transformations. Operating in parallel does not teach operations on multiple threads, and thus does not teach "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads," as recited in claim 16. (Emphasis added).

Operations in parallel also fails to teach a multi-threaded capability, as recited in claim 23. The specification of the present application on page 5 at lines 1-2 states, "Accumulator circuit 100 is a 'multi-threaded' accumulator because it operates on two 'threads' simultaneously." Further, as noted above, the specification of the present invention on page 5, lines 25-26 states, "As a result, the operands on nodes 217 and 218 are interleaved between the sets $\{A_i, B_i\}$ and $\{C_j, D_j\}$."

As argued above with regards to claim 8, Chip *et al.* does not receive interleaved operands at the multiplier. Since Chip *et al.* does not receive interleaved operands (multi-threaded) at the multiplier, Chip *et al.* does not teach the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads, as recited in claim 16, and does not teach multi-threaded capability, as recited in claim 23.

In contrast and as noted above, Chip *et al.* discloses, "arithmetic cores to operate on four ordinate transformations in parallel." Again, a disclosure of "parallel" operations fails to teach the multi-thread operations of the present invention.

Therefore, Chip *et al.* fails the teach each of the elements of claims 16 and 23, and so the

Office Action fails to state a *prima facie* case of anticipation with respect to claims 16 and 23, and also with respect to dependent claims 19-22 that depend from claim 16.

§*103 Rejection of the Claims*

Claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip *et al.* in view of Debabrata *et al.* ("A 600 MHz half-bit level pipelined accumulator-interleaved multiplier accumulator core"). In addition, claims 12-14, 17-18, and 24-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip *et al.* in view Choquette (U.S. 6,480,872).

Applicant respectfully traverses these 35 U.S.C. § 103(a) rejections of claims 10-11 and claims 12-14, 17-18, and 24-30 because the Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-11 and claims 12-14, 17-18, and 24-30.

In each of the above 35 U.S.C. § 103(a) rejections, the Office Action relies on the Chip *et al.* reference to supply the elements of independent claims 8, 16, and 23 used in making the 35 U.S.C. §102 rejection of these claims. However, as discussed in Applicant's previously filed response to a prior Office Action (the prior Office Action mailed February 10, 2005, the previously filed response mailed July 11, 2005), the additional references of Debarate *et al.* and Choquette fail to teach or suggest the elements included in independent claims 8, 16, and 23, and missing from Chip *et al.*

Therefore, the proposed combinations used in forming the 35 U.S.C. § 103(a) rejections of claims 10-11 and claims 12-14, 17-18, and 24-30 fail to teach or suggest all of the elements included in claims 8, 16, and 23 as applied to these claims, and therefore fail to teach or suggest all of the elements included in dependent claims 10-11 and claims 12-14, 17-18, and 24-30, which depend from one of claims 8, 16, and 23 as applied to these claims. Thus, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-11 and claims 12-14, 17-18, and 24-30.

Further, and despite the comments on pages 9-10 in the ***Response to Arguments*** section of the Office Action mailed September 9, 2005 in this application, Applicant maintains that for at least the reasons stated in Applicant's response mailed July 11, 2005, the Office Action fails to state *prima facie* case of obviousness with respect to claims 10-11 by failing to state a proper

basis for forming the proposed combination of Chip *et al.* with Debabrata *et al.*, and with respect to claims 12-14, 17-18, and 24-30 by failing to state a proper basis for forming the proposed combination of Chip *et al.* with Choquette.

Conclusion

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 8-30. Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. Applicant's attorney at (612) 373-6971 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JASON M. HOWARD ET AL.

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date JAN 20/2006 By Robt Madden
Robert Madden
Reg. No. 57,521

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20th day of January, 2006.

Amy Moriarty
Name

Signature